Adaptive CMOS Predistortion Linearizer for Fiber-Optic Links

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***Abstract*—Nonlinearity in the electrical-to-optical conversion limits the dynamic range for transmitting analog and multilevel signals over fiber-optic channels. We describe a complementary metal–oxide–semiconductor (CMOS) predistortion linearizer that extends the dynamic range of both direct and externally modulated links. The linearizer achieves 13–24-dB suppression for both second- and third-order distortions.**

***Index Terms*—Intermodulation distortion, nonlinear distortion, nonlinearities.**

I. Introduction

FIBER-OPTIC links form the backbone of high-speed data communication. With the increase in data rate, dispersion and nonlinearity become critical issues for broad-band data transfer. Multilevel modulation has been considered as a possible solution to fiber impairment (chromatic dispersion and polarization-mode dispersion). Although analog transmission is commercially deployed in cable television (CATV), the cost of devices used in such links is an order of magnitude higher than those used in digital applications. This is mainly because of the stringent linearity specification of electrical-to-optical (E/O) conversion devices, which otherwise are the main source nonlinearity in the link and limits the dynamic range.

Nonlinearity in E/O devices is attributed to the following:

1) static nonlinearity;
2) dynamic nonlinearity;
3) nonlinearity due to overmodulation.

Dynamic nonlinearity is frequency dependent and becomes a dominant source once modulating signal frequency reaches the relaxation oscillation frequency of semiconductor lasers. For Mach–Zehnder-type E/O conversion devices, static nonlinearity, which is due to the inherent nonlinear transfer characteristic of the device, is the dominant source. An analog modulation scheme such as CATV, which operates at less than 1-GHz frequency, is mainly affected with static nonlinearity for both direct and externally modulated links.

Nonlinearity poses severe problems for broad-band data transmission. The modern communication systems try to use more spectral-efficient techniques, increasing the number of channels and reducing the channel bandwidth and channel separation, but the nonlinear effects in the transmitter (mainly the E/O conversion device) form the limiting factor for the spectrum management. Also for the broad-band signal, the peak-to-average power ratio of the transmitted signal is very high and requires a high-dynamic-range transmitter. This makes nonlinearity compensation an attractive solution to improve link performance. Feedforward [1], [2], *post*distortion [3], [4], and predistortion [1], [5], [6] are the most common techniques that offer wide-band linearization. Both feedforward and *post*distortion techniques require additional optical components, which include E/O devices as well, thus, making it a costly solution. Electronic predistortion offers a cost-efficient solution and makes it commercially viable [7].

We present a novel complementary metal–oxide–semiconductor (CMOS) adaptive linearization technique that can be used with both direct and external modulation. The low-cost linearizer can reduce the cost or improve the performance of analog and multilevel optical links. In addition, we discuss the issues involved in achieving broad-band linearization and canceling frequency-dependent dynamic nonlinearities.

This paper starts with a comprehensive analysis of the predistortion linearization principle and the architecture design. The practical circuit implementation issues are also discussed. Next, the optical link setup and adaptive feedback-loop implementation is presented, along with measured performance for directly and externally modulated links.

II. Predistortion Mathematical Analysis

A. System Nonlinearity Modeling

The nonlinear system is modeled as a memoryless system having only second- and third-order nonlinearities. Considering only the predominant second- and third-order nonlinearities, both predistortion and nonlinear systems are modeled using as third-order polynomial transfer characteristics equations [1]. Only the magnitude transfer characteristic is modeled to reduce the complexity of analysis. Fig. 1 shows a mathematical model of the predistortion system, and the predistortion block is placed in cascade with the nonlinear E/O transmitter. The aim of the predistortion block is to introduce the distortion in the input signal such that when it combines with the distortion generated by the nonlinear device, it should cancel out. For the simplicity of analysis, the gain of both blocks is normalized to unity. The aim is to choose the predistortion linearizer coefficient (α, β) so that we have a linear dependence of output

Manuscript received April 15, 2003; revised July 30, 2003. This work was supported in part by the Defense Advanced Research Projects Agency (DARPA).

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Digital Object Identifier 10.1109/JLT.2003.822245

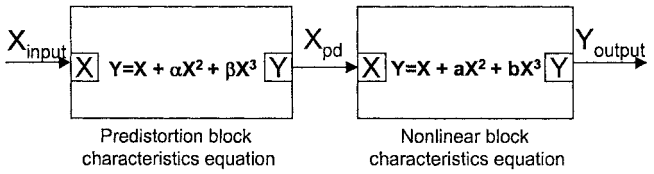

Fig. 1. Predistortion system modeling.

(Y_{output}) on the input signal (X_{input}). Note that the input and output signal ($X_{\text{input}}, Y_{\text{output}}$) are a small signal deviation around bias point. Therefore, the dc-bias term is zero.

The relationship between Y_{output} and X_{input} is expressed as

$$\begin{aligned} Y_{\text{output}} = & X_{\text{input}} + (\alpha + a)X_{\text{input}}^2 + (\beta + 2\alpha a + b)X_{\text{input}}^3 \\ & (3\alpha b + a\alpha^2 + 2\beta a)X_{\text{input}}^4 + \\ & (3b\alpha^2 + 3\beta b + 2\alpha\beta a)X_{\text{input}}^5 + \cdots . \end{aligned} \tag{1}$$

Note that the third-order predistortion block and third-order nonlinear E/O device make the whole system a ninth-order nonlinear device. Since we have only two controllable variables (coefficients α and β), we can reduce at most two coefficients of $X^{\text{n}}(n = 1 \ldots 9)$ to zero in (1). First of all, we note that linearization technique is applied to suppress the nonlinear terms, and this technique is efficient to linearize a system that has predominantly linear gain (i.e., a and $b \ll 1$). In addition, in radio frequency (RF) systems, the input signal amplitude is a small signal ($X_{\text{input}} \ll 1$) quantity. Thus, with the above two assumptions, the contribution by terms $X_{\text{input}}^4, X_{\text{input}}^5 \cdots X_{\text{input}}^9$ can be neglected in (1). The optimum value of α and β (denoted by $\alpha_{\text{opt}}, \beta_{\text{opt}}$) is computed by making the coefficient of X_{input}^2 and X_{input}^3 term zero, as follows:

$$\alpha_{\text{opt}} = -a \tag{2}$$

$$\beta_{\text{opt}} = 2a^2 - b. \tag{3}$$

With the choice of predistortion coefficients obtained by using (2) and (3), we can eliminate of X_{input}^2 and X_{input}^3 terms, but we still have finite contribution from other higher order terms. Now, if the input signal is a pure sinusoid ($X_{\text{input}} = A\sin(wt)$), the fourth- and fifth-order terms will lead to spurious response at second and third harmonic frequencies. Equation (5) gives the expression of output Y_{output} for a sinusoid input signal

$$X_{\text{input}} = A\sin(\omega t). \tag{4}$$

The value of α and β (denoted by $\alpha_{\text{opt}}, \beta_{\text{opt}}$), which completely cancels the spurious response at second and third harmonic frequency, can be computed by solving (6) and (7), as follows:

$$\begin{aligned} Y = & \left[A + \frac{3}{4}(\beta + 2\alpha a + b)A^3 + \frac{10}{16}(3b\alpha^2 + 3\beta b + 2\alpha\beta a)A^5\right]\sin(\omega t) \\ & + \left[-\frac{1}{2}(\alpha + a)A^2 - \frac{1}{2}(3b\alpha + a\alpha^2 + 2\beta a)A^4\right]\cos(2\omega t) \\ & + \left[-\frac{1}{4}(\beta + 2\alpha a + b)A^3 - \frac{5}{16}(3b\alpha^2 + 3\beta b + 2\alpha\beta a)A^5\right]\sin(3\omega t) \end{aligned} \tag{5}$$

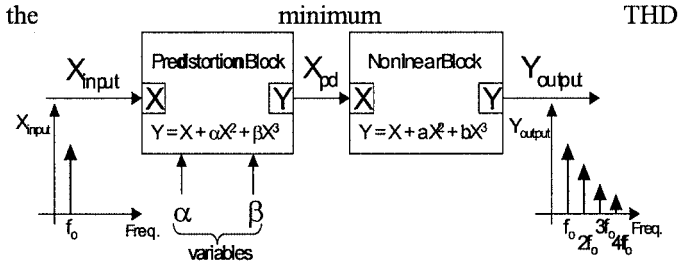

Fig. 2. Predistortion system mathematical simulation model.

$$(aA^2)\alpha^2 + (3bA^2 + 1)\alpha + 2\beta aA^2 + a = 0 \tag{6}$$

$$(15bA^2)\alpha^2 + (10\beta aA^2 + 8a)\alpha + 15\beta bA^2 + 4\beta + 4b = 0. \tag{7}$$

To reduce the complexity, we can neglect the terms "$(aA^2)\alpha^2$" and "$(15bA^2)\alpha^2$, $(10\beta aA^2)\alpha$" in (6) and (7), respectively (assuming that a, b, A, α, and $\beta \ll 1$). The previously mentioned three terms are the multiplication of five factors, where the magnitude of each of the five factors is less than unity. Thus, the magnitude of the neglected terms is very small. With this assumption, we solve (6) and (7). The value thus obtained for α_{opt} and β_{opt} is given by

$$\alpha_{\text{opt}} = -\frac{7abA^2 + 4a}{27bA^2 + 4} \tag{8}$$

$$\beta_{\text{opt}} = -\left(\frac{8a\alpha_{\text{opt}} + 4b}{15bA^2 + 4}\right). \tag{9}$$

The important finding here is that when the assumption of small modulation depth ($A \ll 1$) is no longer valid, the values of α_{opt} and β_{opt} will depend on input signal amplitude (A). An accurate expression can be obtained for α_{opt} and β_{opt} without making the assumptions made in deriving (8) and (9), and it can be shown that the result depends on the modulation depth (A).

B. Effect of Higher Order Terms

The mathematical model shown in Fig. 1 is simulated using Spectre Analog Hardware Description Language (SpectreAHDL). The aim of the simulation is to verify the analytical equation derived for computing α_{opt} and β_{opt} ((2), (3), (8), and (9)). The Spectre simulator provides an optimizing algorithm in which the user can specify the output variable that needs to be optimized (either minimized or maximized) and the tunable input variables upon which this output depends. An arbitrary nonlinear device is chosen, and a pure sinusoid signal is applied to the input of the system. The simulator minimizes the total harmonic distortion (THD) (i.e., the ratio of the sum of powers of all harmonic frequencies above the fundamental frequency to the power of fundamental frequency) at the output by varying the predistortion coefficients (α and β in Fig. 2). The values of α and β, which give the minimum THD at output, correspond to optimum values for achieving maximum linearity. Since this is a mathematical model, the bandwidth is not limited and, hence, all the harmonics are accounted for. Table I summarizes the α and β values obtained by simulation and analytical analysis for four different choices of nonlinear devices with constant input amplitude of 0.2 peak-to-peak ($X = 0.2$).The input amplitude (X) is equivalent to the RF input signal to the CMOS predistortion circuit. In actual implementation, the RF

TABLE I
SIMULATION AND THEORETICAL RESULTS FOR α AND β

Case#	a, b values	Analytical α, β using EQ. (2) & (3)	Simulation result α, β
1	-0.100, -0.050	0.100, 0.070	0.100, 0.06997
2	-0.001, -0.500	0.001, 0.500	0.0012, 0.5041
3	-0.900, -0.001	0.900, 1.621	0.9375, 1.678
4	-0.500, -0.800	0.500, 1.300	0.5269, 1.362

TABLE II
THD OBTAINED FOR THEORETICAL AND SIMULATION α AND β VALUES

Case#	THD at output with theoretical α and β value	THD at output with simulated α and β value
1	-63.09 dB	-63.09 dB
2	-63.09 dB	-63.09 dB
3	-53.92 dB	-61.35 dB
4	-56.23 dB	-62.07 dB

signal amplitude is limited to a couple of tens of millivolts and is capacitively coupled to the predistortion input port with the input dc voltage set at 1.5 V. Thus, $X = 0.2$ corresponds to an equivalent modulation index of 6.7%.

The first case represents a nonlinear device having a modest amount of second- and third-order nonlinearity. The second case is for mainly a third-order nonlinear device. The third one represents the nonlinear device having very high second-order nonlinearity, and the last one is a very nonlinear device with both second- and third-order nonlinearities being high. We see that as the nonlinearity increases, the discrepancy between analytical and simulation values increases because our assumption $(a, b \ll 1)$ is no longer valid.

Table II compares the THD at output for four cases obtained by using analytical and simulation values of α and β. As expected, the last two cases show higher THD value with analytical a and b values. The minimum value of THD (-63.09 dB) was limited by simulation accuracy.

C. Performance of Linearizer With High-Amplitude Input Signal

As seen from the previous analysis, the theoretical optimum value of α and β depends on input signal amplitude (8) and (9); hence, it is important to simulate and find the maximum permissible modulation index. Fig. 3 shows the simulation result for a moderately nonlinear system (with $a = -0.1, b = -0.05$) (note that though the logarithmic x-axis starts from 0.00, the simulation of modulation index starts from a nonzero finite value). Predistortion coefficients are calculated using (2) and (3). THD at output is plotted for two cases, one with linearizer and the other without linearizer. As the modulation index increases, the approximation made $(A \ll 1)$ in (2) and (3) is no longer valid and,

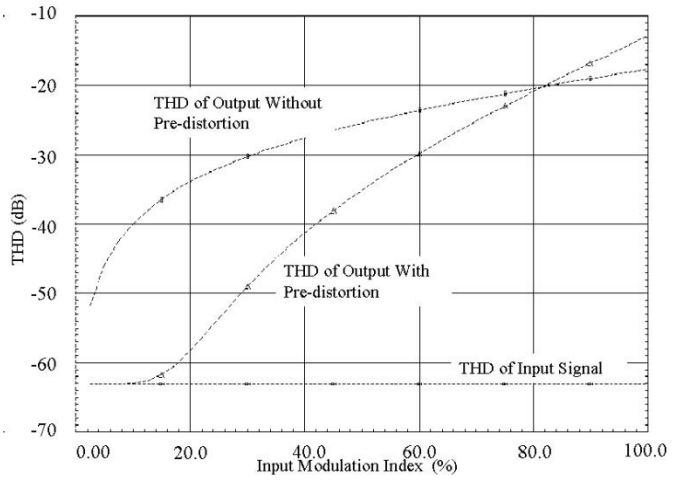

Fig. 3. THD versus input signal modulation index for moderately nonlinear system.

hence, output THD increases even with the linearizer. Thus, to suppress THD at output by 10 dB or more, the modulation index should be less than $\sim 50\%$. Another important observation to be made is that the rate of increase of THD with input signal is higher for predistortion system because the overall system is ninth-order nonlinear (as compared with third-order nonlinear system without the predistortion block). Fig. 4 shows THD for a highly nonlinear system using theoretical predistortion coefficients ($a = -0.5, b = -0.5 => a = 0.5, b = 1$). As seen from the simulation result, for achieving suppression in output THD by more than 10 dB, the modulation index must be less than 10%. Thus, as nonlinearity increases the limit on the maximum input signal, amplitude becomes more stringent.

However, if the predistortion coefficients can be changed with signal amplitude, much higher THD suppression is achieved. Fig. 5 shows the simulation result of such a system, in which predistortion coefficients vary with the input signal bandwidth according to (8) and (9).

Thus, adaptive predistortion coefficient gives much better results. However, such a system will require a feedback loop to control the predistortion coefficients. The bandwidth of the loop will determine the system performance. For a single-carrier system, the required loop bandwidth will depend on the baseband signal bandwidth and is independent of the RF carrier signal. In a subcarrier multiplexing environment (e.g., CATV), the addition of signals with random phase leads to noise like a signal envelope with very high peak-to-average ratio, and the signal envelope can vary with approximately the highest RF carrier frequency, thus requiring a very high bandwidth feedback loop.

The nonlinearity coefficients (i.e., a or b) are typically less than 0.2. For example, in a Mach–Zehnder modulator (MZM) biased at the quadrature point, $a = 0$ and $b = 0.167$. An experiment was carried out to determine the nonlinearity coefficients for a directly modulated laser (ATT SL560) for digital application with a modulation bandwidth of 500 MHz (from 50–500 MHz) and 1-mW optical output power. The coefficients are found to be: $a = 0.02$, $b = 0.13$. Direct-modulated lasers

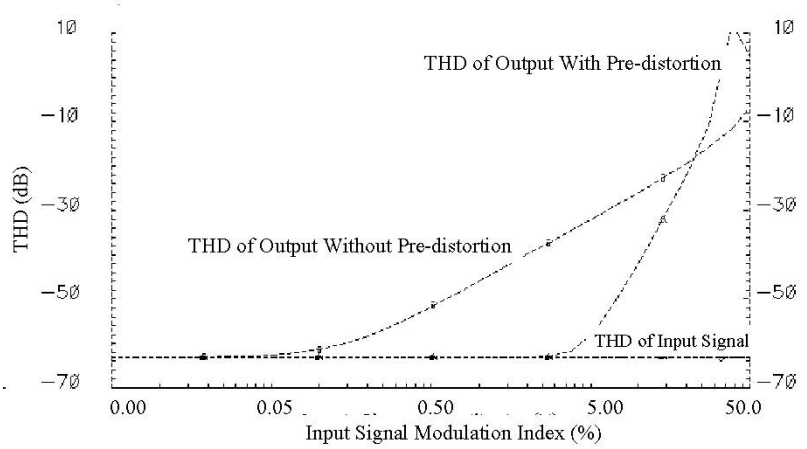

Fig. 4. THD versus input signal modulation index for highly nonlinear system.

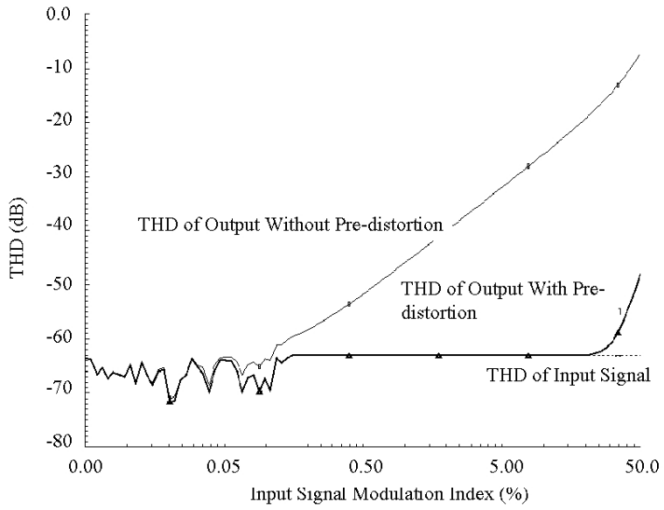

Fig. 5. THD versus input signal amplitude for highly nonlinear system with adaptive predistortion coefficients.

designed for analog application will have even less nonlinear coefficient values. In addition, for CMOS circuits, the input signal amplitude is limited to a couple of tens of millivolts. Under these conditions, predistortion linearization can provide a significant improvement in linearity over a broad frequency bandwidth. Fig. 6 shows the simulated THD for an MZM having nonlinearity coefficients $a = 0.02$ and $b = 0.167$. Note that there is a finite amount of second-order distortion ($a = 0.02$), although theoretically it can be completely cancelled with appropriate biasing [1]. The fixed coefficients predistortion THD is nearly as good as an adaptive coefficient predistortion system for a predominantly linear systems.

D. Predistortion Architecture

A block diagram for the predistortion linearizer system is shown in Fig. 7. The predistortion system has two parts: 1) the predistortion block and 2) the feedback block. The predistortion block generates the nonlinear transfer function required to linearize the E/O device. The feedback controls the predistortion transfer function and provides the adaptive capability.

The architecture for implementing a third-order predistortion function is shown in Fig. 8. This block implements a third-order predistortion polynomial equation. The second- and third-order nonlinear distortion generation (NLG) paths generate harmonics of the input signal with appropriate amplitude and phase. The amplitude and phase of the harmonics is tuned by the feedback block. The feedback-loop monitors the distortion produced at the output of E/O converter and determines the phase and gain coefficient using an appropriate algorithm.

III. Predistortion Circuit Implementation

In the previous section, we introduced a block diagram of the predistortion circuit. The complete system can be partitioned into the following five main components:

1) phase control/adjust block;
2) gain control/adjust block;
3) second-order NLG block;
4) third-order NLG block;
5) adder/output buffer.

To achieve broad-band predistortion, all of these blocks should have a flat frequency response in the signal bandwidth [1]. If the amplitude or phase response is frequency dependent, then the amount of suppression achieved is also variable across the frequency. To take into account the frequency-dependent effects in predistortion system, the mathematical model is modified as shown in Fig. 9, where $\alpha(f)$, $\beta(f)$, $\phi_\alpha(f)$, and $\phi_\beta(f)$ indicate that the gain and phase response of the predistortion block is a function of frequency. For the sake of simplicity, it is assumed that the nonlinear device is wide band with flat frequency response.

To achieve maximum linearization, predistortion coefficients should be chosen as follows:

$$\alpha(f)_{\text{opt}} = a \tag{10}$$

$$\phi_\alpha(f)_{\text{opt}} = 180^\circ + \phi_a \tag{11}$$

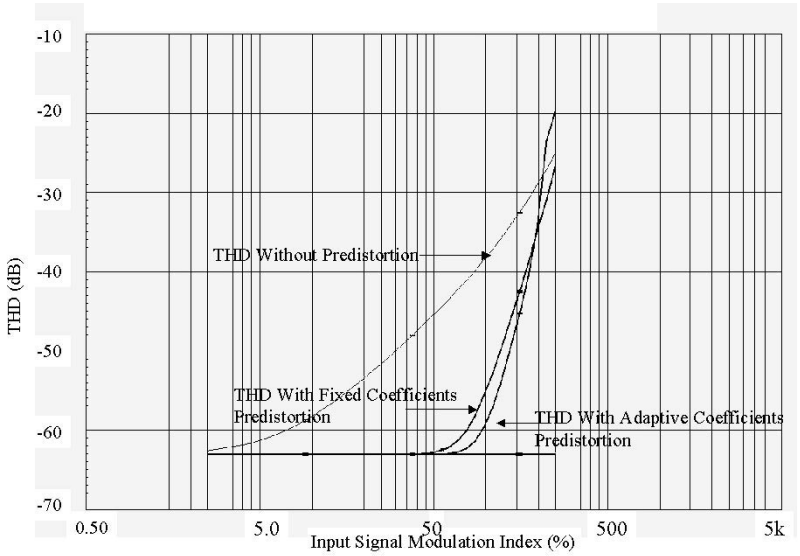

Fig. 6. THD versus input signal modulation index for an MZM having a finite second-order coefficient.

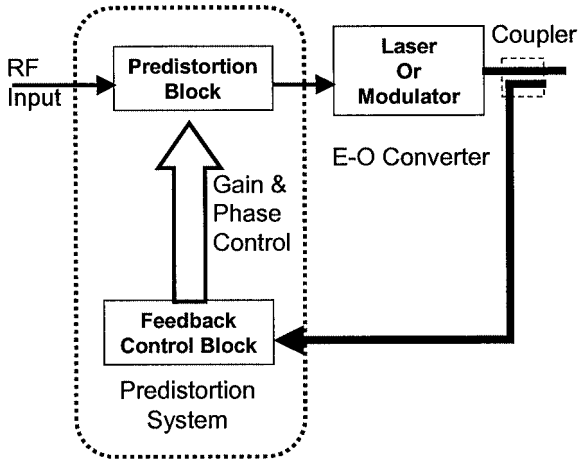

Fig. 7. Adaptive predistortion linearization system architecture.

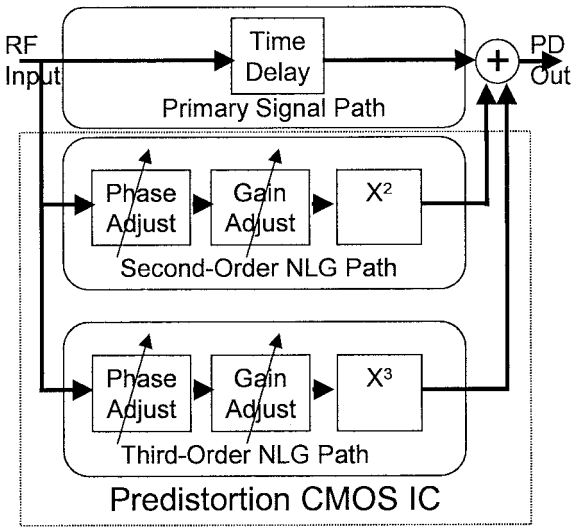

Fig. 8. Predistortion block diagram.

$$\beta(f)_{opt} = \left| \left(2a^2\cos(2\phi_a) - b\cos(\phi_b)\right) + j\left(2a^2\sin(2\phi_a) - b\sin(\phi_b)\right) \right| \tag{12}$$

$$\phi_\beta(f)_{\text{opt}} = 180^\circ + \tan^{-1}\left(\frac{2a^2\cos(2\phi_a) - b\cos(\phi_b)}{2a^2\sin(2\phi_a) - b\sin\phi_b)}\right). \tag{13}$$

If the predistortion coefficients drift from the optimum values, then there would be partial cancellation of distortion components. The above can be looked upon as two phasors, which will cancel each other when their magnitude is the same and the phase differs by 180°, and if any of these criteria is not met, the resultant will be a finite phasor. Fig. 10 shows the amount of suppression theoretically achievable versus the mismatch in gain (Δ_{gain}) (14) and phase (Δ_{phase}) (15) of the phasor.

$$\Delta_{\text{Gain}} = |\alpha(f) - \alpha(f)_{\text{opt}}| \text{ or } |\beta(f) - \beta(f)_{\text{opt}}| \tag{14}$$

$$\Delta_{\text{Phase}} = |\phi_\alpha(f) - \phi_\alpha(f)_{\text{opt}}| \text{ or } |\phi_\beta(f) - \phi_\beta(f)_{\text{opt}}|. \tag{15}$$

To achieve constant suppression across the whole bandwidth, it is desirable to have excess bandwidth in a broad-band linearizer, which will ensure that the correction tones produced by the predistortion circuit experience uniform delay and an equal gain. This requires not only special attention during circuit design, but also efficient layout techniques to minimize parasitic capacitance and inductance, which are the source of droops and ripples in frequency response. In addition, the inevitable gain and phase ripples in the physical implementation make broad-band linearization exceedingly difficult. The design issues and circuit implementation of these blocks using CMOS technology is discussed in the next section.

A. Phase Control Block

This block provides relative phase shift between the primary signal path and distortion generation paths. In effect, it will introduce a relative phase difference between distortions gener-

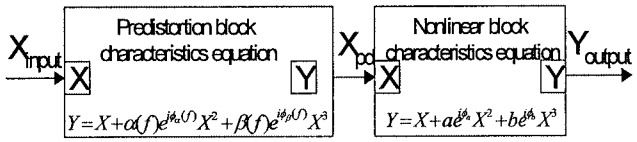

Fig. 9. Predistortion system modeling with frequency-dependent effects.

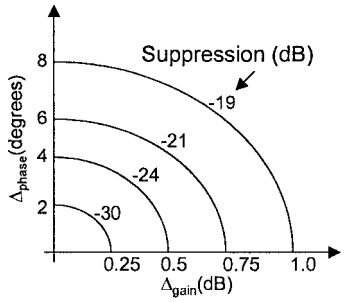

Fig. 10. Effect of amplitude and phase mismatch on the amount of achievable distortion suppression.

ated by the predistortion block and the nonlinear transmitter. The following are two essential specifications for this block:

1) broad-band (signal bandwidth) constant phase difference generation;
2) flat-gain frequency response.

The first criterion will ensure that all the distortion components in the signal frequency band are phase shifted by 180° relative to the distortions generated by E/O device. If the second condition is not satisfied and distortions at a certain frequency band is attenuated or amplified (due to nonflat-gain frequency response), the result would be improper cancellation and finite residual distortions in those frequency bands. A novel architecture to implement the phase control block that satisfies the above two conditions is shown in Fig. 11. A five-stage polyphase filter formed using resistor and capacitor mesh (RC plyphase filter) generates broad-band quadrature signals (I and Q), which are added with a variable gain factor to generate two outputs that have a tunable relative phase angle and a zero relative amplitude variation. Tuning the control voltage scale (κ) from 0 to 1 (the actual can range from 0 to the circuit's supply voltage), the relative phase difference between two outputs can be tuned from 0 to 180° (18).

Since the phase adjust block precedes the distortion generation block, the effective phase tunability for second- and third-order distortion components is more than 360°, as follows:

$$V_{\text{out1}} = \kappa I - (1-\kappa)Q \tag{16}$$

$$V_{\text{out2}} = \kappa I - (1-\kappa)QB = \kappa I + (1-\kappa)Q \tag{17}$$

$$\angle V_{\text{out2}} - \angle V_{\text{out1}} = 2\tan^{-1}\left(\frac{1-\kappa}{\kappa}\right). \tag{18}$$

The bandwidth of the circuit is limited by the polyphase filter frequency response. The filter generates wide-band quadrature signals, but the frequency band in which the amplitude of quadrature signals is the same is determined by the complexity of the filter. A five-stage filter is implemented in commercial 0.18-μm CMOS technology, and it generates an amplitude ripple of less than 0.3 dB in the frequency band of 50 500 MHz across all process corners. Thus, the phase adjust block achieves a decade bandwidth. The measured characteristic of the phase control block is shown in Fig. 12. The control voltage is varied from 0 V to the supply voltage (1.8 V). The measured bandwidth is from 50–450 MHz.

B. Gain Control Block

The gain control block is basically a variable gain amplifier (VGA) that is required to match the amplitude of distortion components generated within the predistortion block to those generated by the nonlinear device. The VGA is cascaded at the output of the phase control block and before the nonlinear distortion block. If the VGA provides gain tunability of χ dB, the gain variation at outputs of the second- and third-order block is 2χ and 3χ, respectively. Thus, placing the VGA before the distortion generation block increases the effective gain tuning range. In addition, it is preferable to have the VGA after the phase delay block, since it relaxes the linearity requirement of phase delay block.

In CMOS technology, the differential amplifier with variable transconductance is a widely used architecture for implementing the VGA [8]. Fig. 13 shows the circuit of the VGA whose transconductance is varied by controlling the bias current of differential amplifier. Since the transconductance of a metal–oxide–semiconductor (MOS) device (g_m) varies as the square root of the bias current (19), so does the gain A_v (20), as follows:

$$g_m = \sqrt{\frac{2\mu C_{\text{OX}} W I_{\text{bias}}}{L}} \tag{19}$$

$$A_V = g_m \times R_{\text{out}} \tag{20}$$

where

g_m transconductance of MOS device (M1,M2);
m mobility;
C_{OX} oxide capacitance;
W, L width and length of MOS device (M1,M2);
I_{bias} bias current for MOS device (M1,M2);
A_v VGA gain;
R_{out} output resistance ($\sim R1, R2$).

The square-root dependence of gain on bias current favors a multistage design for realizing high gain and low power dissipation. The first stage is a VGA whose bias current is varied by control voltage V_{ctrl}, and the second stage is a constant gain stage. Measurements of the fabricated chip show that the VGA achieves a gain tunability of 46 dB (from a minimum gain of -32 dB to a maximum gain of 14 dB).

C. Second-Order Nonlinearity Generation Block

To generate a second-order nonlinear transfer function, the circuit should have a square-law relationship between input and output. This can be easily implemented using a MOS device whose I-V relationship follows square law (21), as follows:

$$I_D = \frac{\mu C_{\text{OX}} W (V_{\text{GS}} - V_t)^2}{2L} \tag{21}$$

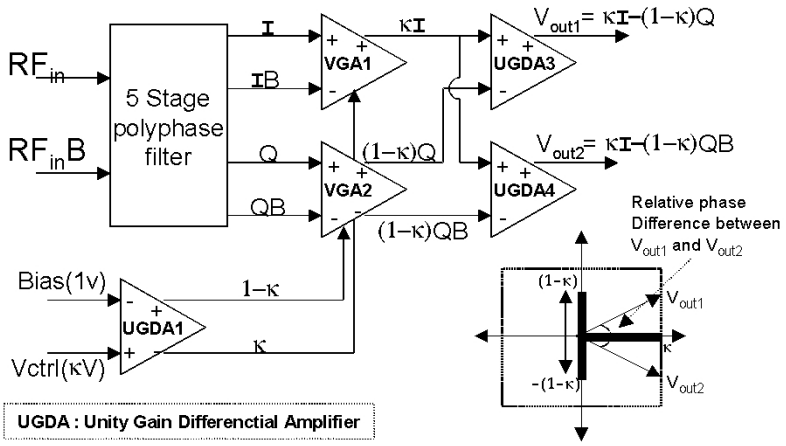

Fig. 11. Phase control block architecture to generate a relative phase difference between primary signal path and distortion generation path.

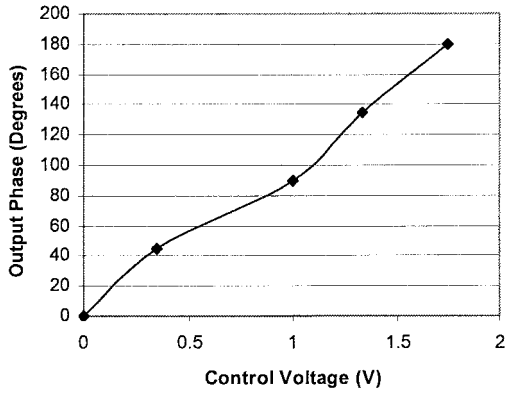

Fig. 12. Phase control block measured characteristic.

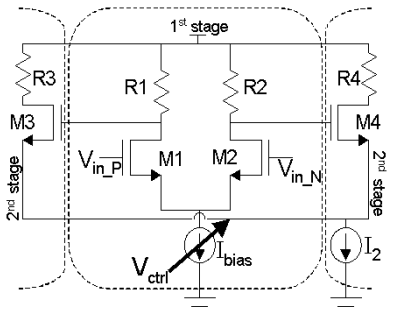

Fig. 13. VGA architecture.

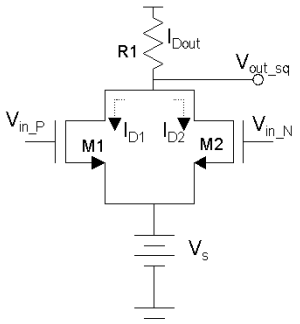

Fig. 14. Two transistor squaring circuit.

where V_t is the threshold voltage of the MOS device. Replacing $V_{\rm GS}$ in (21) by an input ac signal ($v_{\rm i}$) around a dc-bias voltage of $V_{\rm bias}$, the output drain current is given by

$$I_D = K(V_{\rm bias} - V_t)^2 + K(v_{\rm i})^2 + 2K(V_{\rm bias} - V_t)(v_{\rm i}). \quad (22)$$

where $K = \mu C_{\rm OX} W/2L$.

Typically, $v_{\rm i} \ll (V_{\rm bias} - V_t)$; thus, the small-signal output current has a predominantly linear current component ($2K(V_{\rm bias} - V_t)(v_{\rm i})$). If an amplifier is used to amplify the squared input component $(K)(v_{\rm i})^2$, the higher magnitude of the linear component desensitizes the amplifier and limits the gain achieved. In addition, the presence of a significant amount of linear component is undesirable as it will interfere with the signal in the direct feedthrough path and may attenuate the signal. Thus, it is necessary to suppress the linear component at the output, which can be done by implementing a differentially balanced two-transistor squaring circuit [9] (Fig. 14). Assuming both transistors M1 and M2 are perfectly matched and the input signal is fully balanced (around a boas voltage of $V_{\rm bias}$), the output current $I_{D\rm out}$ is given by (23). The output current is converted to voltage by load resistance R1, thus providing a square-law dependence of the output voltage on the input signal voltage.

$$I_{D\rm out} = I_{D1} + I_{D2} = 2K(V_{\rm bias} - V_S - V_t)^2 + 2K(v_{\rm i})^2. \quad (23)$$

The following are the two most important design considerations for achieving desired performance:

1) matching between MOS devices M1 and M2;
2) overcoming the short channel effects in MOS transistors.

To achieve better matching, the device size is kept large [10], and layout is done using multi-finger common-centroid geometry to cancel the process gradient. To overcome the short channel effect, the device length should be large, and a low gate-to-source bias voltage is desirable. Fig. 15 shows the measured characteristics of this block. As seen from the graph, the fundamental tone is suppressed to the same level as the second-order tone. Ideally, the distortion generator's output should not have any component at the fundamental frequency. However, relative to the power from the primary path of the predistortion circuit (Fig. 8), the fundamental-frequency power observed in Fig. 15 is negligible and, hence, will not affect the linearizer's operation.

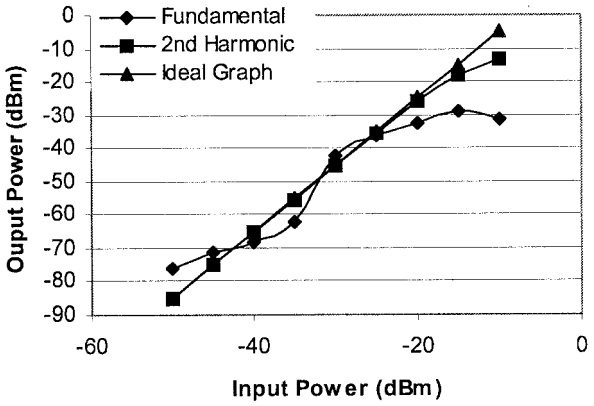

Fig. 15. Measured response of the second-order nonlinearity generation block.

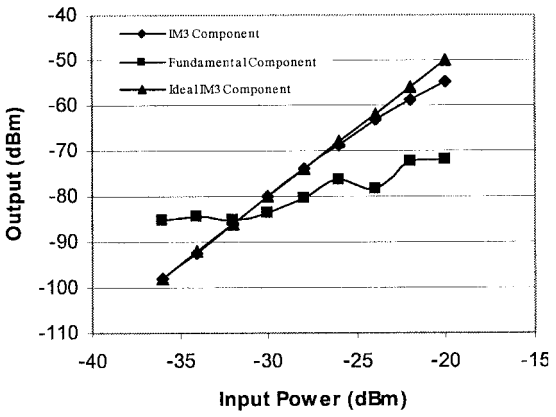

Fig. 17. Measured response of third-order nonlinearity generation block.

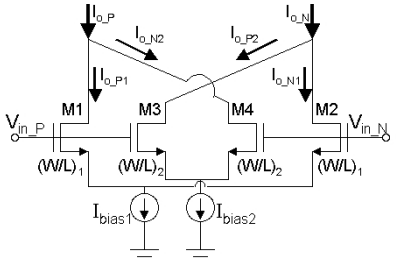

Fig. 16. Cross-coupled differential pair (CCDP) architecture to cancel the fundamental component and leave only third-order nonlinearity in the circuit. Fully differential architecture ensures cancellation of even-order components.

D. Third-Order Nonlinearity Generation Block

Third-order distortion generation block has cubic input–output relationship and can be implemented using the translinear circuit principle [11]. A fully balanced translinear cubic law circuit uses approximately 24 MOS devices, all of which must be matched and free of short-channel effects. This renders the implementation sensitive to process and supply variations. A circuit employing the least number of devices is preferable to achieve higher bandwidth and reducing process-related mismatches. One such circuit is a cross-coupled differential pair (CCDP) [12]. Ordinarily, the CCDP is used to cancel the odd-order nonlinearities in the differential amplifier; however, as it will be shown subsequently, it can be an effective architecture to synthesize a cubic transfer function. For a common-source biased differential pair (bias current $I_{\rm bias}$), the differential output current ($I_{\rm diff}$) and input signal voltage ($V_{\rm diff}$) are related by

$$I_{\rm diff}=\sqrt{\frac{\mu C_{\rm OX}WI_{\rm bias}}{L}}V_{\rm diff}-\frac{1}{8}\sqrt{\frac{1}{I_{\rm bias}}\left(\frac{\mu C_{\rm OX}W}{L}\right)^3}V_{\rm diff}^3. \tag{24}$$

Equation (24) neglects terms higher than third order. We note that increasing W/L and reducing $I_{\rm bias}$ will increase the third-order component. Since the minimum value of $I_{\rm bias}$ is limited by the bandwidth requirement, and $V_{\rm diff}\ll 1$ V, the magnitude of the linear component is much higher than that of the third-order component. The CCDP shown in Fig. 16 consists of two differential pairs. The differential output current from the CCDP is $I_{\rm out}=I_{\rm O\_P}-I_{\rm O\_N}=I_{\rm out1}-I_{\rm out2}$, where $I_{\rm out1}=I_{\rm O\_P1}-I_{\rm O\_N1}$ and $I_{\rm out2}=I_{\rm O\_P2}-I_{\rm O\_N2}$. Since W/L and the bias current are different for both differential pairs, the following condition ensures that the linear component of the output current is cancelled:

$$\left(\frac{W}{L}\right)_1 I_{\rm bias1}=\left(\frac{W}{L}\right)_2 I_{\rm bias2} \tag{25}$$

resulting in the cubic transfer function

$$I_{\rm out}=-\sqrt{\frac{(\mu C_{\rm OX})^3}{64K_{\rm O}}}\left[\left(\frac{W}{L}\right)_1^2-\left(\frac{W}{L}\right)_2^2\right]V_{\rm diff}^3. \tag{26}$$

In practice, the cancellation of the linear component is not perfect. Nonetheless, the measurement transfer function of the fabricated circuit shows that the circuit primarily exhibits a third-order behavior (Fig. 17). Again, the observed amount of the linear component is not of concern since it is negligible compared with that contributed by the fundamental path of the predistortion circuit (Fig. 8).

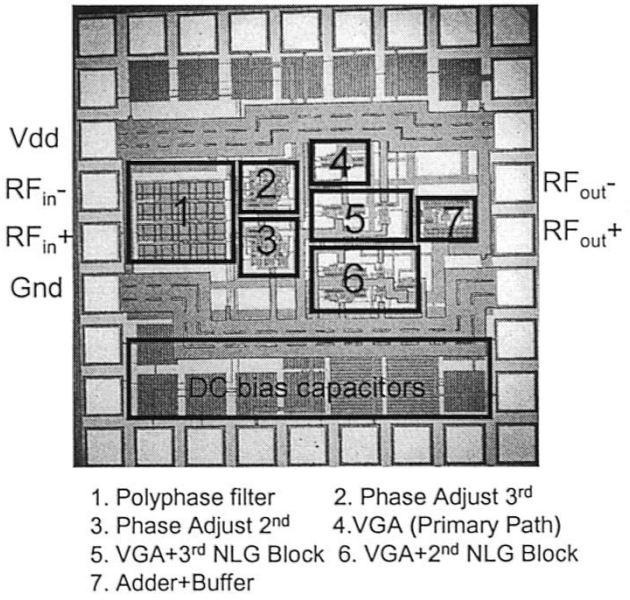

Fig. 18. Predistortion chip micrograph: 0.18-μm technology; area = 1.32 × 1.32 μm; power consumption = 162 mW.

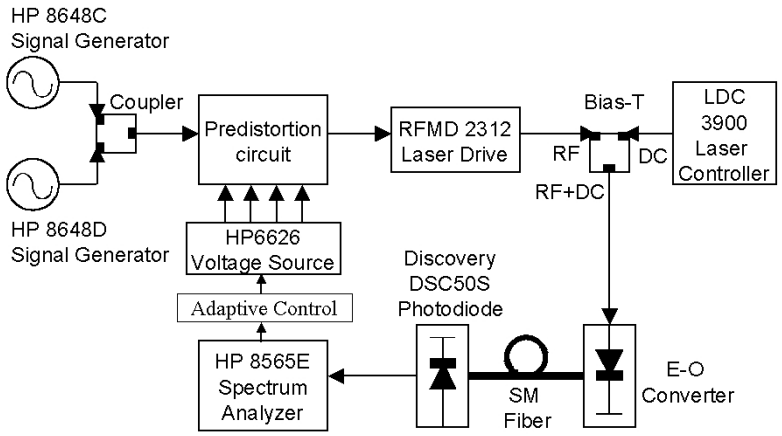

Fig. 19. Optical link setup to measure the performance of predistortion circuit for linearizing the characteristic of E/O convertor.

E. Adder/Output Buffer

The output signal from all three paths is converted to the current using differential transcoductance amplifiers, and the resulting output currents are added in a common 50-Ω load. The same block also provides a 50-Ω output impedance.

The predistortion circuit is fabricated in 0.18-μm CMOS technology. The chip micrograph shown in Fig. 18 occupies a 1.32 $\times$ 1.32-mm area and consumes 90 mA from a 1.8- V supply.

IV. Optical Link Setup and Measurement Results

A. Optical Link Setup

An optical link is set up to characterize the performance of predistortion circuit. Fig. 19 shows the complete test setup. A two-tone signal was applied to the predistortion circuit. The output RF signal from predistortion is fed to a laser driver integrated circuit (IC) (RFMD2312). The predistortion circuit performance is tested with direct and external modulation. Second- and third-order distortions are measured using the spectrum analyzer. The feedback mechanism that controls the gain and the phase of the predistortion circuit is described in the next section. A precision supply source (An HP6626) was used to adjust the phase and amplitude of second- and third-order distortion components according to the signal provided by the feedback control mechanism.

B. Feedback Control Loop

The purpose of the feedback loop is to minimize the second- and third-order distortion at the link output by tuning predistortion gain and phase control signals. The feedback loop, shown in Fig. 20, is set up using a PC equipped with a data acquisition card and Labview software.

The algorithm implemented to reach an optimum solution is designed to find the global minima of output intermodulation (IM) power by varying the amplitude and phase control voltages. Since the dependence of output IM power on amplitude and phase control voltages is not a known function, the algorithm sweeps both the voltages (from minimum to maximum value) in coarse steps to narrow down the voltage ranges for successive iterations. Measurements show that convergence

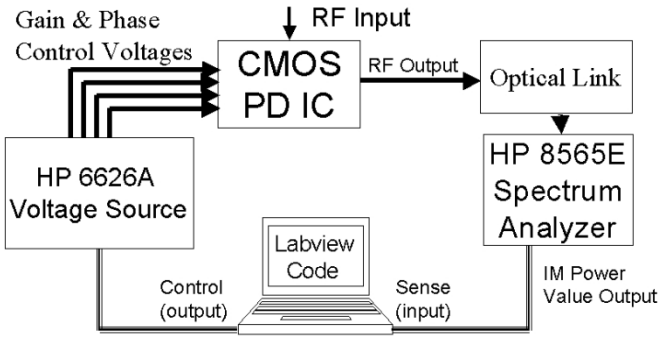

Fig. 20. Feedback-loop implementation.

is achieved in four iterations, where each iteration partitions the amplitude and phase control voltage range in ten linear step sizes. The resolution of the voltage source (1.5 mV for the HP6626A) is also a determining factor for the maximum achievable IM suppression.

Fig. 21 shows the third-order IM power versus phase and amplitude control voltage for the coarse iteration. The amplitude control voltage adjusts the gain of the VGA. The amplitude control voltage is varied from 0.5–1.05 V. The minimum voltage is set by the threshold voltage of the n-channel MOSFET implemented to generate the I_{bias} in Fig. 13, and the maximum voltage is set by the current limit of the VGA. The narrow voltage tuning range achieves faster convergence at the expense of increased sensitivity to unwanted voltage fluctuations. The phase control voltage is varied from 0 to the supply voltage (1.8 V).

Once convergence is reached for coarse iteration, the software performs a fine iteration to reach the global minima. Fig. 21 also shows the reduction in IM3 power during the fine iteration.

C. Link Spurious Free Dynamic Range Measurement

The predistortion performance is tested with the following four different E/O devices:

1) direct modulation with a high-linearity distributed feedback (DFB) laser;
2) direct modulation with a low-cost DFB laser;
3) external modulation with an MZM;

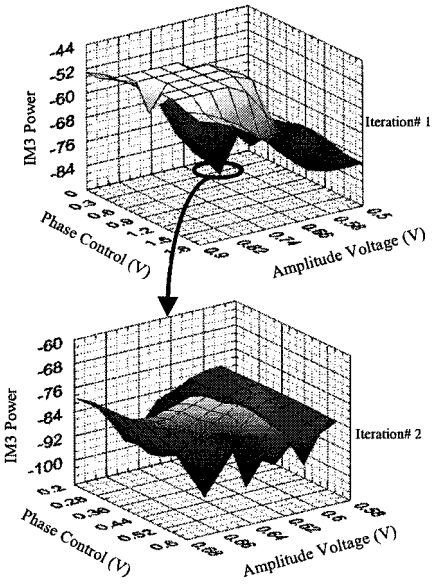

Fig. 21. IM3 power versus phase and gain control voltage curves generated by the feedback loop.

4) external modulation with an electroabsorption modulator (EAM).

1) Direct Modulation With a High-Linearity DFB Laser: The Fujitsu FLD5F7CZH laser is a highly linear DFB laser designed for analog applications. This laser provides higher link spurious free dynamic range (SFDR); however, it has a high cost compared with DFB lasers used in digital communication. Fig. 22 shows that the predistortion circuit is able to further increase the dynamic range of this laser. The third-order intercept point (IIP3) is determined by carrying out two-tone tests for various input power values. The IM3 suppression due to the predistortion circuit is measured for a 50-MHz system bandwidth. The measured noise floor (RIN-limited) and IIP3 value is used to find the link SFDR in Fig. 22.

The SFDR improved by 5.5 dB (from 105.8 to 111.3 dB-Hz2/3). Improvement in SFDR is measured for various IM3 tone separation (i.e., system bandwidth, discussed in Section IV-D) while keeping the center frequency around 250 MHz. The adaptive feedback loop renders the system tolerant to laser temperature variations. Fig. 23 shows that the IM3 suppression remains almost constant with variation in DFB laser temperature over 15–35°C, which is done by changing thermoelectric cooler (TEC) current from the minimum to the maximum permissible value.

At the optimum bias point, second-order distortion is not a concern. In particular, measurements show that when the bias current is more than twice the threshold current, the link is third-order distortion limited [12]. To demonstrate the capability of the predistortion circuit to simultaneously minimizing second- and third-order nonlinearities, the laser is biased such that both IM2 and IM3 are significant. Fig. 24 shows the reduction in both IM2 and IM3 products. Fig. 25 shows SFDR_2 plots with 6.5-dB improvement in IIP2 with the predistortion circuit. A high IIP2 value makes system SFDR limited by the third-order distortion component.

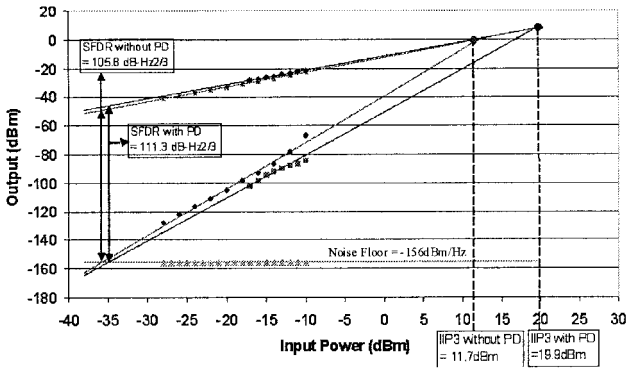

Fig. 22. SFDR improvement with predistortion circuit for Fujitsu FLD5F7CZH laser.

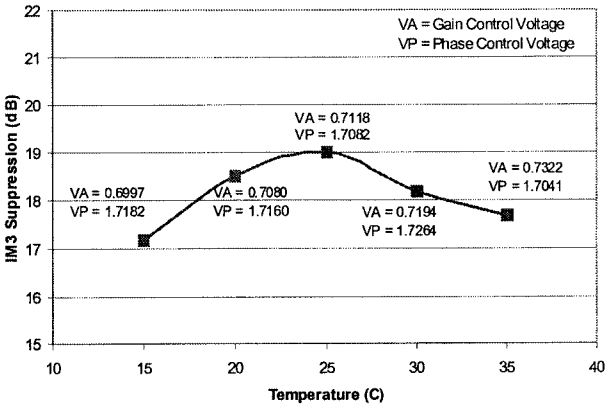

Fig. 23. IM3 suppression at various DFB laser temperatures. Adaptive feedback loop changes the gain and phase control voltages of the predistortion circuit in order to track the changes in transfer characteristics of the laser with changes in its operating temperature.

2) Direct Modulation With Low-Cost DFB Laser: The predistortion circuit is used to measure the improvement in the SFDR of a low-cost DFB laser used for digital applications. The AT&T SL560 has a wavelength of 1550 nm and is designed for 622-Mb/s communication. Measurements were performed over a system bandwidth of 50 MHz centered at 250 MHz. The predistortion circuit achieves more than 20-dB suppression of IM3. Consequently, the link SFDR improves by 8 dB, from 80 to 88 dB-Hz2/3.

3) External Modulation With an MZM: The link is tested with a $LiNbO_3$ MZM using a 1550- nm continuous-wave (CW) laser source. As is well known, the second-order distortion of the MZM can be minimized by biasing the device at the quadrature bias point. Fig. 26 shows strong dependence of IM2 on bias voltage, whereas IM3 does not show much variation. The adaptive feedback loop is used to obtain the optimum bias point by minimizing IM2, rendering the link IM3 limited. The predistortion circuit then minimizes the IM3 distortion. As shown in Fig. 27, the predistortion circuit achieves more than 18-dB IM3 suppression and improves the link SFDR by 6.2 dB, i.e., from 95.1 to 101.3 dB-Hz2/3.

4) Optical Link Using an EAM: The predistortion circuit is tested with the EAM (Cyoptics 1010) designed for digital modulation. As shown in Fig. 28, predistortion improves

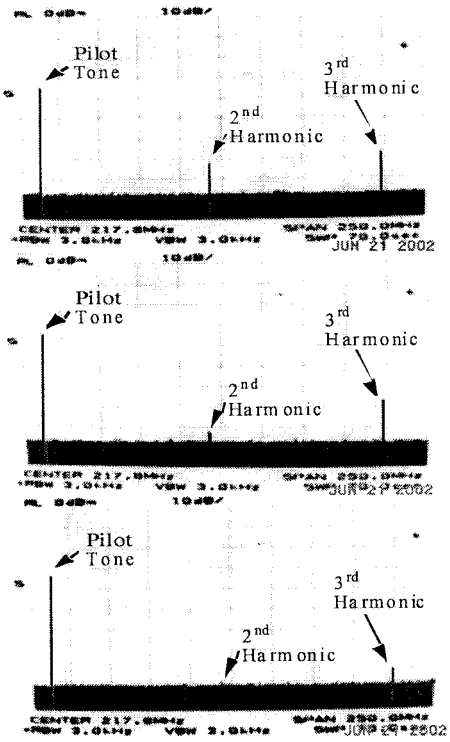

Fig. 24. Top plot shows the result without the predistortion circuit (pilot tone = 105 MHz, 2ndHarmonic = 210 MHz, 3rdHarmonic = 315 MHz). The center plot shows reduction in second harmonic by predistortion circuit; the bottom plot shows that both second- and third-harmonics are reduced.

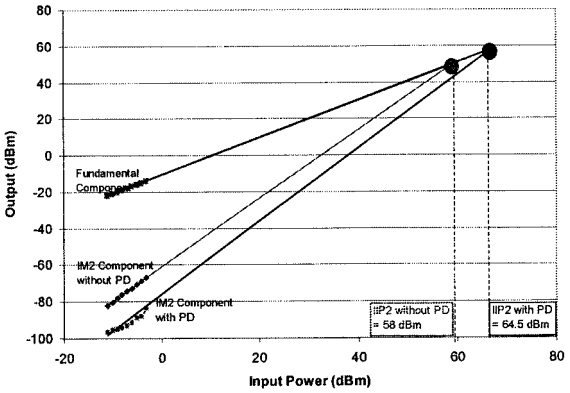

Fig. 25. IIP2 improvement by predistortion circuit. An IM2 suppression of 13.0 dB and an IIP2 improvement of 6.5 dB is achieved with the predistortion circuit.

the IM3-limited SFDR of the link by 6.0 dB (from 95.2 to 101.2 dB-Hz2/3). The second-order distortion component was found to be strongly dependent on the bias voltage of the EAM. Thus, the feedback loop is used to reduce the second-order distortion. At this bias point, the EAM was found to show finite second-order distortion, which did not show any predictable dependence on the input signal power. Thus, it also could not be reduced by predistortion circuit.

D. Predistortion Circuit Performance and System Bandwidth

One very important performance criterion of the linearizer is the bandwidth over which it can suppress the distortion components. This bandwidth is measured as the frequency difference between two IM3 components in two-tone tests. Measurements show that the dynamic range degrades with an increase in the

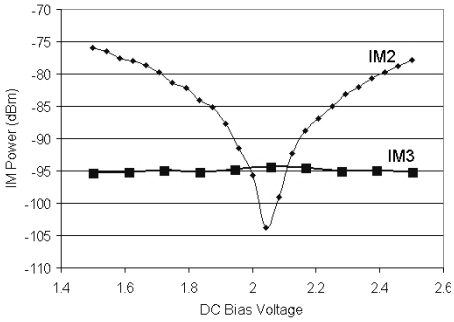

Fig. 26. IM3 and IM2 dependence on bias voltage of $LiNbO_3$ modulator. IM2 shows strong dependence on bias voltage and can be reduced significantly by appropriate bias-voltage selection.

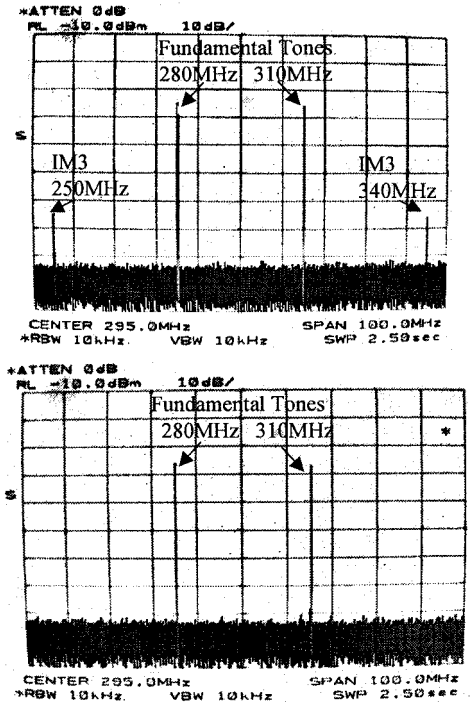

Fig. 27. IM3 suppression for externally modulated link employing $LiNbO_3$ MZM. Predistortion circuit achieves 18-dB IM3 suppression (lower spectrum) for a system bandwidth of 90 MHz (IM3 tone frequencies = 250 and 340 MHz).

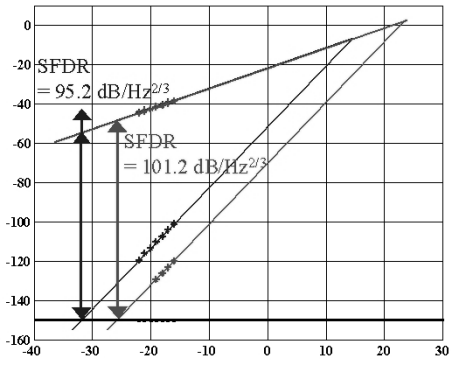

Fig. 28. SFDR improvement with predistortion circuit for EAM (Cyoptics).

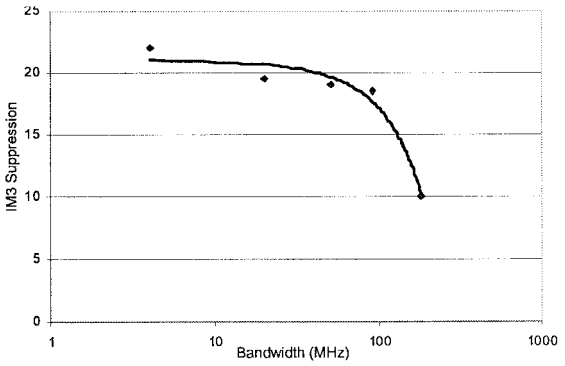

Fig. 29. IM3 suppression versus system bandwidth for externally modulated links ($LiNbO_3$ MZM). An IM3 suppression of 22.1 dB at 6-MHz bandwidth reduces to 9.8-dB suppression at 180-MHz bandwidth (with center frequency at 295 MHz).

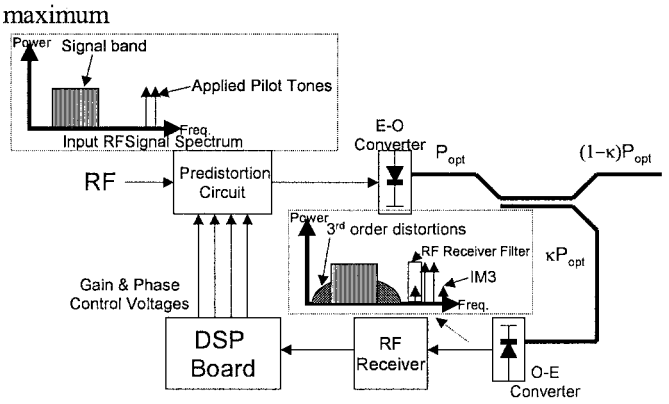

Fig. 30. Feedback-loop setup using RF receiver and DSP board. The RF receiver filters out the IM component, and the DSP board runs the algorithm to determine the predistortion coefficients.

system bandwidth beyond 90 MHz. The reason is that upper and lower IM3 tones do not show equal suppression, and the spectrum becomes lopsided for large bandwidths. In order to have the same suppression over the entire bandwidth, the feedback loop sets the predistortion coefficients so that both IM3 tones have the same power. This reduces the amount of suppression at higher bandwidths. As shown in Fig. 29, an IM3 suppression of 22.1 dB at 6-MHz bandwidth reduces to 9.8-dB suppression at 180-MHz bandwidth for externally modulated links employing a $LiNbO_3$ MZM. The direct-modulated DFB laser also shows similar behavior. We have identified the nonuniform frequency response of the link as the origin of this behavior. This frequency response has two sources: 1) the inherent nonuniform phase response of the E/O device and 2) impedance mismatches in the experimental setup. Circuit and system simulation using the experimentally measured phase response of E/O device confirmed the former to be the source of bandwidth limitation. The latter can be alleviated with improved packaging, while the former must be addressed by the linearizer IC. This can be done by introducing a frequency tilt filter before and after the predistortion circuit. The filter can be implemented on chip with a predistortion circuit to provide a single-chip solution. One very common filter class suitable for this application is the tunable tapped delay-line filter, which is often used in communication transmitters and receivers to complement the frequency response of the communication channel.

V. Discussion

The present link setup used a PC with data acquisition card to form the adaptive feedback loop for the link. In order to increase the loop settling time, the complete feedback loop can be realized using an RF receiver (to detect IM power) and a programmable digital signal processor (DSP) to implement the algorithm. Fig. 30 shows such a system. A fraction (κ) of the optical power is fed to the feedback loop, and the RF receiver filters out the desired IM component (either IM3 or IM2) and outputs an analog signal proportional to IM power. This signal is converted to digital and is processed by the DSP algorithm which, in turn, sets the predistortion phase and gain control voltages.

The problem of linearization consists of two parts: 1 the predistortion of the input signal and 2) the detection of the IM products at the output. The purpose of this paper has been to describe the design and performance of a CMOS linearizer IC, capable of increasing the dynamic range of both directly modulated and externally modulated optical links. While a detailed discussion of IM detection is beyond the scope of this paper, we do provide a brief discussion of this problem hereafter and highlight one recently proposed solution for an important problem which is real-time detection of IM distortion.

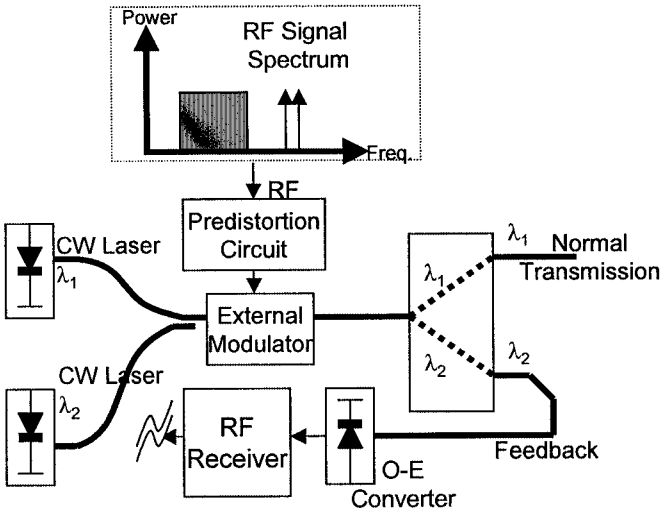

Fig. 31. Improved feedback architecture to increase the feedback coupling coefficient (k) to unity.

The following are three possibilities for measuring IM distortions:

1) measuring out-of-band IM distortions;
2) measuring IM components generated by a pilot tone signal;
3) the wavelength-division-multiplexing (WDM) pilot tone technique.

A. Measuring Out-of-Band IM Distortion

In this scheme, the RF receiver filters the IM3 distortion near the signal band and measures the amount of third-order nonlinearity. This technique does not require a pilot tone signal and is capable of monitoring IM3 distortion continuously without the need to interrupt normal signal transmission to calibrate the

predistortion. However, for a highly linear link, the distortion power is very weak, rendering the detection extremely difficult.

B. Measuring IM3 Generated by Two-Tone Test Signal

This scheme, also shown in Fig. 30, filters the IM3 component of the two-tone test signal applied in the presence of the actual data signal. The pilot tone power can be adjusted independent of the input signal such that there is sufficient distortion power at the RF receiver. However, distortion caused by pilot-signal beating will limit the maximum dynamic range that can be achieved with such a technique [14]. To mitigate this problem, the pilot tone can be applied during an initial calibration phase and in periodic intervals when necessary. For application where the transfer function of the E/O device changes rapidly, this approach will not be adequate. Such systems require real-time detection of IM power and continuous-time adaptivity of the predistortion circuit. One possible enabling approach is the recently proposed WDM pilot technique [15], summarized hereafter.

C. WDM Pilot Tone Technique

Referring to Fig. 30, if the coupling factor (κ) could be increased to unity, then pilot IM distortion power can be increased at the RF receiver without increasing the pilot-signal IM power in the link. Typically, the coupling factor is limited to approximately 1 or 2% in order not to reduce the link power [14]. A novel technique that can solve this problem in externally modulated links is the WDM pilot tone technique, shown in Fig. 31 [15]. Here, a separate laser is used for detecting the distortion power. The WDM demux redirects all the power of the pilot laser to the feedback loop. Consequently, the pilot tone RF power can be kept low such that the pilot-signal IM distortion does not limit the link dynamic range. The dependence of the modulator's bias on wavelength results in nonoptimum bias at the signal wavelength. Hence, there will be residual IM2 in the link [15]. To minimize this and maintain an IM3-limited performance, the signal-pilot wavelength spacing cannot be very large. The wavelength dependence of the bias point in an MZM and the resulting dependence of SFDR have recently been quantified by Dubovitsky *et al*. [16]. In the context of the WDM pilot tone technique, the results suggest that the required wavelength spacing is in the range of 2–4 nm, depending on the desired SFDR [15]. Such wavelength spacings are well within the capability of commercial WDM lasers and filters.

VI. Conclusion

We presented the first monolithic predistortion IC solution capable of 1) simultaneously reducing both second- and third-order nonlinear distortion, 2) linearizing both direct (DFB laser) and externally modulated (MZM and EAM) links, and 3) an adaptive capability eliminating the need of manual fine-tuning and offering supply and temperature tolerant operation. The linearizer achieves 13–24-dB suppression for second- and third-order distortions. Table III summarizes the measurement result obtained for various kinds of E/O conversion devices. System analysis and measurements show that the nonidealities in the frequency response of E/O conversion device limit the IM suppression bandwidth. This problem can be alleviated with the addition of a frequency-shaping filter to the predistortion circuit. In addition, to cancel the second- and third-order distortions completely, there is need for either increasing the order of the predistortion circuit or implementing the adaptive coefficient predistortion circuit. The latter scheme also helps to achieve linearization at higher modulation index.

TABLE III
PREDISTORTION IC PERFORMANCE WITH DIFFERENT E/O DEVICES

E-O Converter	Without Predistortion	With Predistortion	Improvement (dB)
Fujitsu FLD5F7CZH	IIP3=11.7dBm	IIP3=19.9 dBm	8.2
direct modulated laser	IIP2=58 dBm	IIP2=64.5 dBm	6.5
for analog application	SFDR=105.8 dB-Hz$^{2/3}$	SFDR=111.3 dB-Hz$^{2/3}$	5.5
ATT SL 560 direct	IIP3=-9.5 dBm	IIP3=2.5 dBm	12.0
modulated DFB laser	IIP2=32 dBm	IIP2=39.5 dBm	7.5
for digital application	SFDR=80 dB-Hz$^{2/3}$	SFDR=88 dB-Hz$^{2/3}$	8.0
LiNbO3 modulator +	IIP3=-2.5 dBm	IIP3=6.8 dBm	9.3
JDSU CQF 938 laser	SFDR=95.1 dB-Hz$^{2/3}$	SFDR=101.3 dB-Hz$^{2/3}$	6.2
Cyoptics EAM1010	IIP3=14.5 dBm	IIP3=23.5 dBm	9.0
EAM modulator	SFDR=95.2 dB-Hz$^{2/3}$	SFDR=101.2 dB-Hz$^{2/3}$	6.0

Acknowledgment

The authors would like to thank B. Schneider for his support and J. Basak for performing the EAM measurements.

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